REGISTERED DDR SDRAM DIMM

D21RB2GZT – 2GB 36 chips
D27RB2GZT – 2GB 36 chips
D32RB2GZT – 2GB 36 chips

For the latest data sheet, please visit the Super Talent Technology web site: www.supertalent.com

Features

- VDD : 2.5V ± 0.2V, VDDQ : 2.5V ± 0.2V for DDR266, 333
- VDD : 2.6V ± 0.1V, VDDQ : 2.6V ± 0.1V for DDR400
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4)
- Differential clock inputs(CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency : DDR266(2, 2.5 Clock), DDR333(2.5 Clock), DDR400(3 Clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM
- SSTL_2 Interface
- 60 ball FBGA

Figure 1: 184-Pin DIMM
36 chip memory module designs

30.48 mm

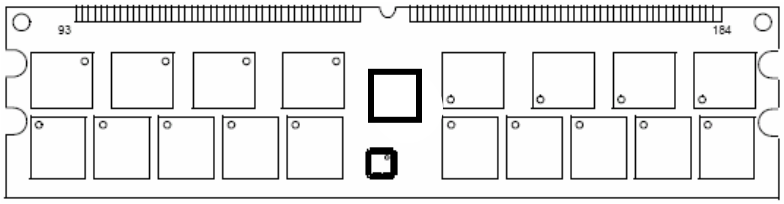


Table 1: Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD},V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5 * # of component	W
Short circuit current	Ios	50	mA

Note :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Table 2: Pin Descriptions

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~ DM8	Data - in mask
BA0 ~ BA1	Bank Select Address	VDD	Power supply (2.5V for DDR266/333, 2.6V for DDR400)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS (2.5V for DDR266/333, 2.6V for DDR400)
DQS0 ~ DQS17	Data Strobe input/output	VSS	Ground
CK0,$\overline{CK0}$	Clock input	VREF	Power supply for reference
CKE0, CKE1(for double banks)	Clock enable input	VDDSPD	Serial EEPROM Power/Supply (2.3V to 3.6V)
$\overline{CS0}$, $\overline{CS1}$(for double banks)	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0 ~ 2	Address in EEPROM
WE	Write enable	VDDID	VDD, VDDQ level detection
CB0 ~ CB7	Check bit(Data-in/data-out)	NC	No connection

Note: VDDID defines relationship of VDD and VDDQ, and the default status of it is open (VDD = VDDQ)

Table 3: Pin Configuration (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0/DQS9	128	VDDQ	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3/DQS12	159	DM5/DQS14
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	$\overline{RESET}$	41	A2	71	*$\overline{CS2}$	102	NC	133	DQ31	163	*$\overline{CS3}$
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	N/C	106	DQ13	137	CK0	167	*A13
15	VDDQ	46	VDD	76	N/C	107	DM1/DQS10	138	$\overline{CK0}$	168	VDD
16	N/C	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6/DQS15
17	N/C	48	A0	78	DQS6	109	DQ14	140	DM8/DQS17	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7/DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2/DQS11	149	DM4/DQS13	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

Note:

1. * : These pins are not used in this module
2. Pins 111, 158 are NC for 1row module & used for 2row module
3. Pins 97, 107, 119, 129, 140, 149, 159, 169, 177 : DQS (x4 base module).

Figure 2: Functional Block Diagram – 2GB

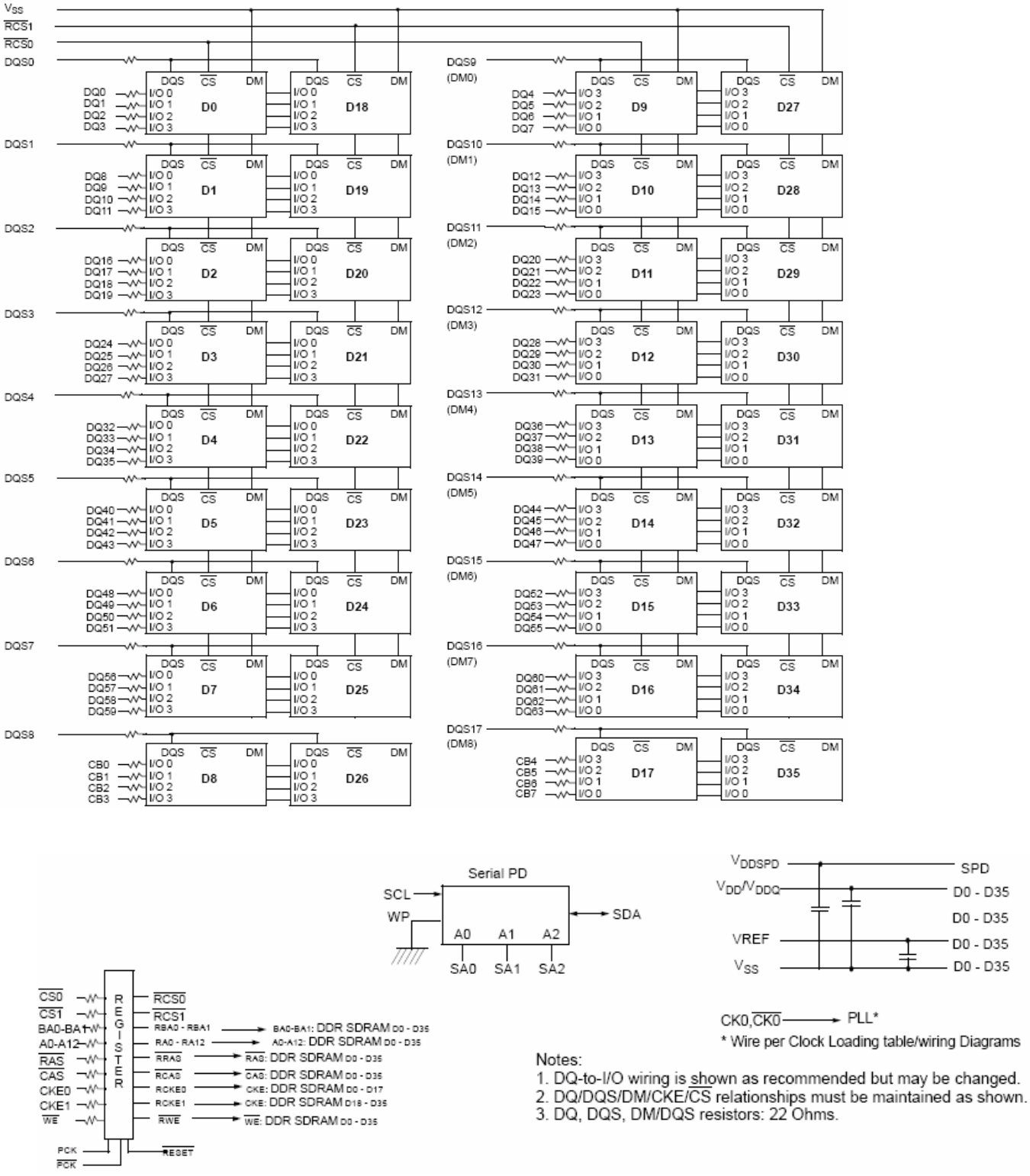


Table 4: Command Truth Table (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	CS	RAS	CAS	WE	BA0,1	A10/AP	A0 ~ A9 A11, A12	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address (A0~A9, A11,A12)		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note :
1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

Table 5: Power & DC Operating Conditions (SSTL_2 In/Out)

Recommended operating conditions (Voltage referenced to Vss=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V for DDR266/333)	V_{DD}	2.3	2.7	V	
Supply voltage(for device with a nominal V_{DD} of 2.6V for DDR400)	V_{DD}	2.5	2.7	V	
I/O Supply voltage(for device with a nominal V_{DD} of 2.5V for DDR266/333)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage(for device with a nominal V_{DD} of 2.6V for DDR400)	V_{DDQ}	2.5	2.7	V	
I/O Reference voltage	V_{REF}	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.36	V_{DDQ}+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Note :

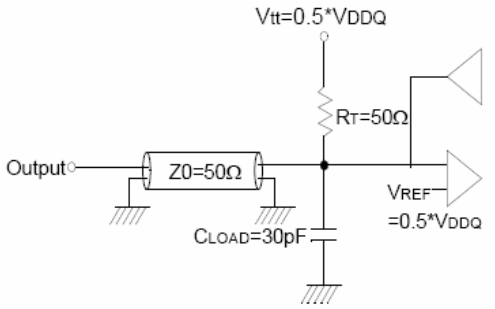
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
3. VID is the magnitude of the difference between the input level on CK and the input level on CK.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

Table 6: AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :

1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.



Output Load Circuit (SSTL_2)

Table 7: Input/Output Capacitance

(TA = 25°C, f = 100MHz)

Parameter	Symbol	M312L6523BT(U), M312L2920BT(U)		M312L2923BT(U) M312L5720BT(U)		Unit
		Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN1	9	11	9	11	pF
Input capacitance(CKE0)	CIN2	9	11	9	11	pF
Input capacitance($\overline{CS0}$)	CIN3	9	11	9	11	pF
Input capacitance(CLK0, $\overline{CLK0}$)	CIN4	11	12	11	12	pF
Input capacitance(DM0~DM8)	CIN5	10	11	14	16	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	10	11	14	16	pF
Data input/output capacitance (CB0~CB7)	Cout2	10	11	14	16	pF

Parameter	Symbol	M312L6523BG(Z), M312L2920BG(Z)		M312L2923BG(Z), M312L5720BG(Z)		Unit
		Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN1	9	11	9	11	pF
Input capacitance(CKE0)	CIN2	9	11	9	11	pF
Input capacitance($\overline{CS0}$)	CIN3	9	11	9	11	pF
Input capacitance(CLK0, $\overline{CLK0}$)	CIN4	11	12	11	12	pF
Input capacitance(DM0~DM8)	CIN5	10	11	13	15	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	10	11	13	15	pF
Data input/output capacitance (CB0~CB7)	Cout2	10	11	13	15	pF

Table 8: AC Timing Parameters & Specifications

Parameter		Symbol	CC (DDR400@CL=3.0)		B3 (DDR333@CL=2.5)		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5)		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	55		60		65		65		ns	
Refresh row cycle time		tRFC	70		72		75		75		ns	
Row active time		tRAS	40	70K	42	70K	45	70K	45	70K	ns	
RAS to CAS delay		tRCD	15		18		20		20		ns	
Row precharge time		tRP	15		18		20		20		ns	
Row active to Row active delay		tRRD	10		12		15		15		ns	
Write recovery time		tWR	15		15		15		15		ns	
Last data in to Read command		tWTR	2		1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	-	-	7.5	12	7.5	12	10	12	ns	
	CL=2.5		6	12	6	12	7.5	12	7.5	12	ns	
	CL=3.0		5	10	-	-	-	-	-	-		
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.55	+0.55	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.4	-	0.45	-	0.5	-	0.5	ns	22
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.72	1.28	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		0		ns	13
DQS-in hold time		tWPRE	0.25		0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		0.35		tCK	
Address and Control Input setup time(fast)		tIS	0.6		0.75		0.9		0.9		ns	15, 17~19
Address and Control Input hold time(fast)		tIH	0.6		0.75		0.9		0.9		ns	15, 17~19
Address and Control Input setup time(slow)		tIS	0.7		0.8		1.0		1.0		ns	16~19
Address and Control Input hold time(slow)		tIH	0.7		0.8		1.0		1.0		ns	16~19
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	11
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	11
Mode register set cycle time		tMRD	10		12		15		15		ns	
DQ & DM setup time to DQS		tDS	0.4		0.45		0.5		0.5		ns	j, k
DQ & DM hold time to DQS		tDH	0.4		0.45		0.5		0.5		ns	j, k
Control & Address input pulse width		tIPW	2.2		2.2		2.2		2.2		ns	18
DQ & DM input pulse width		tDIPW	1.75		1.75		1.75		1.75		ns	18
Exit self refresh to non-Read command		tXSNR	75		75		75		75		ns	
Exit self refresh to read command		tXSRD	200		200		200		200		tCK	
Refresh interval time		tREFI		7.8		7.8		7.8		7.8	us	14
Output DQS valid window		tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	21
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	20, 21
Data hold skew factor		tQHS		0.5		0.55		0.75		0.75	ns	21
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	12
Active to Read with Auto precharge command		tRAP	15		18		20		20			
Autoprecharge write recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	23

Component Notes and System Notes:

11. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
12. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.
13. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previ ously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
14. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
15. For command/address input slew rate ≥ 1.0 V/ns
16. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
17. For CK & CK slew rate ≥ 1.0 V/ns
18. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
19. Slew Rate is measured between VOH(ac) and VOL(ac).
20. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
21. tQH = tHP - tQHS, where: tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p channel to n-channel variation of the output drivers.
22. tDQSQ - Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
23. tDAL = (tWR/tCK) + (tRP/tCK) For each of the terms, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3) tDAL = 5 clocks

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. The delta rise/fall rate is calculated as: {1/(Slew Rate1)} – {1/(Slew Rate2)} For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . This would result in the need for an increase in tDS and tDH of 100 ps.

k. Table is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC - AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

Figure 3: 184-Pin DIMM Dimensions – 2GB

Units : Millimeters